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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

02079358.4

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
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Failsafe method and circuit

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Failsafe method and circuit

The present invention relates to a failsafe method and circuit for producing a failsafe output signal in case of an open circuit condition of an input pad of a digital circuit unit.

An undesired behavior at the system level occurs in case of unconnected input pins. If these input pins would be allowed to float this will lead to undesired switching of the output due to thermal noise. To prevent thermal noise switching an open failsafe mechanism is added. The open failsafe mechanism is activated only if the input pins are not connected. The open fail safe mechanism pulls an input terminal of a disconnected cable to a defined level when an open circuit (invalid signal level) is detected. The open failsafe mechanism prevents undesired behavior at the system level in case of unconnected input pins. Several options are possible: comparators, diodes, MOSFETs or high threshold input stages.

The open failsafe mechanism is used in low voltage differential signaling (LVDS) products. In LVDS small differential signals are used to transport data information. The applicable standard is TIA/EIA-644. The standard TIA/EIA-644 says that other standards and specifications using the electrical characteristics of a LVDS interface circuit may require that specific interchange circuits be made failsafe to certain fault conditions. Such fault conditions may include one or more of the following, like generator in power-off condition; receiver not connected with the generator; open-circuited interconnecting cable; short-circuited interconnecting cable; input signal to the load remaining within the transition region (±100 mV) for an abnormal period of time (application dependent). When detection of one or more of the above fault conditions is required by specified applications, additional provisions are required in the load and the following items must be determined and specified: which interchange circuits require fault detection; what faults must be detected; what action must be taken when a fault is detected, the binary state that the receiver assumes; what is done does not violate this standard. The method of detection of fault conditions is application dependent and is therefore not further specified as it is beyond the scope of this standard.

US 6,288,577 B1 discloses a fail-safe circuit for a differential receiver which can tolerate high common-mode voltages. An output from a differential amplifier that receives a V+ and a V- differential signal can be blocked by a NOR gate when the fail-safe condition is detected, such as when the V+, V- lines are open. Pull up resistors pull V+, V- to VCC when an open failure occurs. A pair of comparators receive a reference voltage on the non-inverting input. Once comparator outputs a high when the V+ line is above the reference voltage, and the other comparator outputs a high when the V- line is above the reference voltage. When both V+ and V- are above the reference voltage, the NOR gate blocks the output from the differential amplifier, providing a fail-safe. Since the reference voltage is very close to VCC, a high common-mode bias can exist on V+, V- without falsely activating the fail-safe circuit.

US 6,288,577 B1 uses a failsafe circuit which pulls input lines to VCC in case of open lines. Further, it utilizes an analog comparator to compare one of the differential signals V+ and V- with a reference voltage that equals 97% of VCC. Furthermore, bipolar transistors may be required to get the required performance from the comparator.

US 6,320,406 B1 discloses an active fail-safe method and apparatus for a LVDS receiver that uses a window comparator circuit to monitor the differential voltage at the receiver's input pins and drive the output to a known logic HIGH state in the absence of a valid input signal; i.e., when the input differential signal is less than a chosen threshold value of approximately 80 mV. Such a condition may occur when the cable is removed or damaged in such a way that no valid input signal is present. In the presence of a valid input signal, the circuit's output tracks the differential input without any degradation to the signal.

The US 6,320,406 B1 describes a LVDS receiver that detects too small differential voltage and blocks input. By means of a pull resistor between both differential inputs A and B both input voltages are drawn to each other in an open situation. The window comparator checks if this signal difference drops below 80 mV. The comparator is an analog circuit, it incorporates bipolar transistors and it requires at least one reference current source A described timer prevents direct influence of the open failsafe on the output signal. If the timer would be omitted, the open failsafe detection would be activated at every signal transition.

It is the object of the present invention to provide a failsafe method and circuit for producing a failsafe output signal in case of an open circuit condition of an input pad of a digital circuit unit.

To achieve the object of the present invention a method for producing a failsafe output signal in case of an open circuit condition of an input pad of a digital circuit unit is disclosed comprising providing a constant switch level in a first inverter stage providing a variable switch level in the second inverter stage that depends of the signal level of the input pad; comparing the constant switch level of the first inverter stage to the variable switch level of the second stage and providing an output signal at an output terminal thereof if the switch level of the second stage is greater than the constant switch level; and decreasing the switching level of the second inverter stage by an additional circuit element in series with the second inverter, whereby a defined output is produced irrespective of the open circuit condition of an input pad.

To achieve the object of the present invention a failsafe circuit for producing a failsafe output signal in case of an open circuit condition of an input pad of a digital circuit unit is disclosed, comprising a first inverter stage providing a constant switch level; a second inverter stage providing a variable switch level that depends of the signal level of the input pad and comparing the constant switch level of the first inverter stage to the variable switch level of the second stage and providing an output signal at an output terminal thereof if the variable switch level of the second stage is greater than the constant switch level; and an additional circuit element in series with the second inverter for decreasing the switching level of the second inverter stage.

The advantageous features of the method and the circuit are that there is no need for current mirrors, bandgaps, or other analog parts. The present invention is simple to implement, because hardly any tuning is needed. It is easy to simulate and to match on a lay-out. The spent die area is very small. The process dependency is reduced. Simulations showed that the switch level varies hardly with process parameter variation.

According to a preferred embodiment of the invention, the first inverter stage is a transistor stage, and wherein the gate terminals and the drain terminals of the transistors of the first inverter stage are connected to each other.

According to a preferred embodiment of the invention, the second inverter stage is a transistor stage, and wherein the gate terminals of the transistors of the second inverter stage are connected to each other and wherein the drain terminals of the transistors are connected to each other.

According to a preferred embodiment of the invention, the gate terminals of the second inverter stage are connected to the gate terminals of the first inverter stage.

According to a preferred embodiment of the invention, the input terminal is connected to a source terminal of the second inverter stage.

According to a preferred embodiment of the invention, the output terminal is connected to a drain terminal of the second inverter stage.

According to a preferred embodiment of the invention, the additional circuit element is a transistor in saturated mode.

According to a preferred embodiment of the invention, the additional circuit element is a transistor in saturated mode where the gate of the transistor is connected to the VCC and the source is connected to ground whereby the defined signal is a high level signal.

According to a preferred embodiment of the invention, the additional circuit element is a transistor in saturated mode where the gate of the transistor is connected to the ground and the source is connected to VCC whereby the defined signal is a low level signal.

To achieve the object of the present invention a digital circuit unit is disclosed comprising an input terminal, a pull-up circuit, a failsafe circuit, a signal processing circuit and an output terminal, wherein the failsafe circuit comprises the features mentioned above.

These and various other advantages and features of novelty which characterize the present invention are pointed out with particularity in the claims annexed hereto and forming a part hereof. However, for a better understanding of the invention, its advantages, and the object obtained by its use, reference should be made to the drawings which form a further part hereof, and to the accompanying descriptive matter in which there are illustrated and described preferred embodiments of the present invention.

Fig. 1 shows a block diagram of the present invention;

Fig. 2 shows a circuit diagram of the present invention, whereby the switch level is close to VCC;

Fig. 3 shows a circuit diagram of the present invention, whereby the switch level is close to GND;

Fig. 4 shows a circuit diagram of an application of the present invention;

Fig. 5 shows an input signal and the corresponding output signals demonstrating the effect of the present invention.

Fig. 1 shows a block diagram of the present invention. The block diagram comprises an input pad connected to an input of a pull-up network 2 and to an input terminal of a failsafe stage 4. The output of the pull-up network 2 as connected to the input of the failsafe stage 4. The output of the failsafe stage 4 is connected to an input terminal of a signal processing stage 6. Several other signals are supplied to the signal processing stage 6. The signal processing stage 6 provides an open circuit failsafe signal at its output.

If the input pad is not connected an thus floating, the voltage level is being pulled to VCC by the pull-up network 2. The pull-up network 2 can be either a resistor or a transistor connected to VCC. The failsafe stage 4 detects whether the input signal has a defined signal level and switches in case of a not defined signal level to VCC or to GND depending on the application. The failsafe stage 4 provides in case of a floating input signal a defined signal level to the signal processing stage 6. After that an open circuit situation is detected or not, the output signal of the failsafe stage 4 is processed in the signal processing stage 6 together with other output signals of failsafe stages or internal signals.

Fig. 2 shows a circuit diagram of the present invention. The shown circuit diagram has a switch level close to VCC. The circuit diagram comprises a resistance 8 connected on one side to VCC and on the other side to a source terminal 12 of a transistor 10. The transistor 10 is a p-MOSFET. A gate contact 14 of transistor 10 is connected to a gate contact 22 of transistor 18. The transistor 18 is a n-MOSFET transistor. A drain contact 16 of transistor 10 is connected to a drain contact 20 of transistor 18. A source terminal 24 of transistor 18 is connected to a resistance 26. The resistance 26 is connected on the other side to ground. The gate terminals 14 and 22 are connected to the drain terminals 16 and 20. The substrate terminal 30 of transistor 10 is connected to VCC. An input terminal 28 is connected to a source terminal 36 of a transistor 32. The transistor 32 is a p-MOSFET. A substrate terminal 38 of transistor 32 is connected to the input terminal 28. A gate terminal 34 of transistor 32 is connected to the drain terminals 16 and 20 and to the gate terminals 14 and 22. The gate terminal 34 is connected to a gate terminal 48 of a transistor 44. The transistor 44 is a n-MOSFET. A drain terminal 40 of transistor 32 is connected to an output terminal 42 and to a source terminal 46 of transistor 44. A source terminal 50 of transistor 44 is connected to a drain terminal 54 of transistor 52. The transistor 52 is a n-MOSFET. A gate terminal 56 of transistor 52 is connected to VCC. A source terminal 58 of transistor 52 is connected to ground.

The operation of the circuit of Fig. 2 is described in the following text. Assume that the Nwell resistors 8 and 26 are shorted. The drains 16 and 20 and gates 14 and 22 of the transistors 10 and 18 are all connected to each other. This results in a stable situation where both the transistor 10 and the transistor 18 are open and the voltage of the drains 16 and 20 and the gates 14 and 22 remains at a constant voltage. This is defined as the "specific switch level" for this combination of the p-MOSFET 10 and the n-MOSFET 18 at this specific supply voltage ($V_{SP|VCC}$).

Transistor 32 and transistor 44 have the same dimensions as the transistors 10 and 18 have respectively. The gates 34 and 48 of the transistors 32 and 44 are also connected to the drains 16 and 20 and the gates 14 and 22, so that this switch level is also applied on the gates 34 and 48 of the transistors 32 and 44. However, at the source 36 of transistor 32 is not VCC but the input signal 'inl'.

Now, assume that drain and source of transistor 52 are shorted in the circuit. The specific switch level for transistor 32 and transistor 44 is named $V_{SP|INI}$ and has exactly the same value as for the transistors 10 and 18 ($V_{SP|VCC}$). When 'inl' starts to rise, the specific switch level $V_{SP|INI}$ increases for the combination of the transistor 32 and the transistor 44. Nevertheless, this level does not exceed $V_{SP|VCC}$, and thus the output 'out1' remains at low voltage, because $V_{SP|VCC}$ can be considered as 'high' input voltage on the gates of transistor 32 and transistor 44.

When 'in1' finally reaches the same level as VCC, the $V_{SP|VCC}$ equals $V_{SP|in1}$. The voltage at the drains 16, 20 and gates 14, 22, 34, 48 can now be considered as a 'low' input signal on the gates of transistor 32 and transistor 44 and therefore the output 42 switches from GND to VCC.

Now, the transistor 52 is included in the circuit. The gate 56 of transistor 52 is connected to VCC, resulting in an actuated n-MOSFET, that will work like a diode (i.e. in saturation a voltage of $V_{DS.transistor52}$ drops across this transistor 52 in combination with a constant current). This voltage drop is defined as $V_{SD.transistor52}$. This causes the $V_{SP|in1}$ to decrease (defined as $V_{SP|in1}'$), resulting that the condition $V_{SP|in1}' < V_{SP|in1}$ is achieved before in1 reaches VCC. The extra voltage drop between the gate 48 and source 50 of transistor 44 causes this decrease in switch level. The channel length of transistor 52 has an effect on the switch level. If the gate length of transistor 52 is increased, $V_{SD.transistor\ 52}$ will also increase resulting in a higher $V_{GS.transistor\ 44}$ and thus lowering the switch level even more. For our application, the switch level was 0.3 Volts below VCC.

The resistors 8 and 26 are placed to reduce static current. The combination of transistor 10 and transistor 18, are conducting quite some current in this operation mode. These resistors can be tuned into the circuit to meet with the products ICC specification. However, these resistors 8 and 26 can have some influence on the switch level and process dependency of the switch level.

Fig. 3 shows a circuit diagram of the present invention. The shown circuit has a switch level close to GND. The circuit comprises a resistance 60 connected on one side to VCC. The resistor 60 is connected on the other side to a source terminal 64 of a p-MOSFET transistor 62. A substrate terminal 65 of transistor 62 is connected to VCC. A gate terminal 66 of transistor 62 is connected to a gate terminal 74 of transistor 70. A drain terminal 68 of transistor 62 is connected to a drain terminal 72 of transistor 70 and to the gate terminal 66 and to the gate terminal 74. A source terminal 76 is connected to a resistance 78. The resistance 78 is connected on the other side to GND. A source terminal 82 of a p-MOSFET transistor 80 is connected to VCC. A substrate terminal 88 of transistor 80 is also connected to VCC. A gate terminal 84 of transistor 80 is connected to GND. A drain terminal 86 of transistor 80 is connected to a source terminal 92 of a p-MOSFET transistor 90. A substrate terminal 92 of transistor 90 is connected to VCC. A gate terminal 96 of transistor 90 is connected to the drain terminals 68 and 72 and to the gate terminals 66 and 74. The gate terminal 96 is also connected to a gate terminal 104 of a n-MOSFET transistor 100. A drain terminal 98 of transistor 90 is connected to an output terminal 108 and to a drain terminal 102 of transistor 100. A source terminal 106 is connected to an input terminal 110.

The operation of the circuit shown in Fig. 3 is analogue to the operation of Fig. 2. The circuit in Fig. 3 has a switch level close to GND. This circuit can be used in combination with a pull-down network.

The cells depicted in Fig. 2 and 3 can detect whether the input signal lies close to one of the supply rails. Close can be specified as a certain offset that is introduced by transistor 52 (Fig. 2) or transistor 80 (Fig. 3). It depends on the application whether the circuit of Fig. 2 or of Fig. 3 is used. For an application when there is an open circuit occurrence and the signal should be pulled close to VCC, so the circuit of Fig. 2 applies for this case. For an application when there is an open circuit occurrence and the signal should be pulled close to GND, so the circuit of Fig. 3 applies for this case. An advantageous feature of the present invention is that only five transistors are used for the failsafe part.

Fig. 4 shows an application of the present invention. Fig. 4 comprises a differential signal stage 120 connected to the input terminals 112 and 114. A resistance 116 is

connected on one side to VDD and on the other side to the input terminal 114. A resistance 118 is connected on one side to VDD and on the other side to the input terminal 112. The input terminal 112 is connected to an inverter 126. An output terminal of inverter 126 is connected to an input terminal of a logic gate 130, for example a NAND gate. An input terminal of the inverter 126 is connected to an output terminal of an inverter 124. The output terminal of the inverter 124 is connected to an input terminal of the inverter 124. The two inverters 124 and 126 represent the circuit of Fig. 2 or Fig. 3. Inverter 124 represents for example the two transistors 10 and 18 of Fig. 2. Inverter 126 represents for example the transistors 32, 44 and 52. The connection of the input terminal of inverter 124 to the output terminal of the inverter 124 and to the input terminal of inverter 126 represents the connection between the drain terminals 16 and 20 and the gate terminals 14, 22, 34 and 48. The output terminal of inverter 126 represents the output terminal 42. The input terminal of inverter 126 connected to the input terminal 112 represents the input terminal 28 of Fig. 2. The input terminal 114 is connected to an inverter 128. The inverter 128 is connected to an inverter 127 in the same way as the inverter 126 is connected to the inverter 124. The inverters 127 and 128 represent in principle the same circuit as the inverters 124 and 126. The output terminal of the inverter 128 is also connected to a logic gate 130. The logic gate 130 combines the output signals the inverter 126 and the inverter 128. The output of the logic gate 130 is connected to an output unit 122. The output terminal of the inverter 120 is also connected to the output unit 122. The output unit 122 combines the output signals of the inverter 120 and of the logic unit 130 and provides a common output signal.

The embodiment of Fig. 4 uses the present invention in combination with the pull-up resistors 116 and 118. If the resistors 116 and 118 are large enough, this will have no influence on the normal operation.

By using the source 36 of the p-MOSFET 32 of an inverter as in input terminal, it is no longer required to have an extreme small p-MOSFET over n-MOSFET ratio. A small imbalance in the stage suffices to arrive at a threshold level with an offset from VCC. The outputs of a first failsafe stage comprising inverter 124 and inverter 126 and of a second failsafe stage comprising the inverters 127 and 128 are connected to the input terminals of the logic gate 130 that combines the output signals and, if required, brings the output in the open failsafe condition.

The present invention can be implemented for example in a high speed differential line receiver that implements the electrical characteristics of Low Voltage Differential Signaling (LVDS). LVDS is used to achieve higher data rates on commonly used

media. LVDS overcomes the limitations of achievable slew rates and electromagnetic interference (EMI) restrictions of previous differential signaling techniques.

Fig. 5 shows an input signal and the corresponding output signals for three different cases. The first case is the normal case. In the normal case every input pin has a defined input voltage. The output signal corresponds to the input signal.

The second case shows the output signal in case of a floating input value without a failsafe stage of the present invention. The output signal shows an unexpected signal which is completely useless.

The last case shows an output signal, where at least one input signal is floating and the failsafe stage of the present invention is used. The third case shows the example, where the signal is drawn to a high level leading to an useable output signal.

New characteristics and advantages of the invention covered by this document have been set forth in the foregoing description. It will be understood, however, that this disclosure is, in many respects, only illustrative. Changes may be made in details, particularly in matters of shape, size, and arrangement of parts, without exceeding the scope of the invention. The scope of the invention is, of course, defined in the language in which the appended claims are expressed.

CLAIMS:

1. A method for producing a failsafe output signal in case of an open circuit condition of an input pad of a digital circuit unit comprising:

providing a constant switch level in a first inverter stage;

providing a variable switch level in the second inverter stage that depends of the signal level of the input pad;

comparing the constant switch level of the first inverter stage to the variable switch level of the second stage; and

providing an output signal at an output terminal thereof if the switch level of the second stage is greater than the constant switch level; and

decreasing the switching level of the second inverter stage by an additional circuit element in series with the second inverter,

whereby a defined output is produced irrespective of the open circuit condition of an input pad.

2. A failsafe circuit for producing a failsafe output signal in case of an open circuit condition of an input pad of a digital circuit unit, comprising:

a first inverter stage providing a constant switch level;

a second inverter stage providing a variable switch level that depends of the signal level of the input pad and comparing the constant switch level of the first inverter stage to the variable switch level of the second stage and providing an output signal at an output terminal thereof if the variable switch level of the second stage is greater than the constant switch level; and

an additional circuit element in series with the second inverter for decreasing the switching level of the second inverter stage.

3. The circuit of claim 2, wherein the first inverter stage is a transistor stage, and wherein the gate terminals and the drain terminals of the transistors of the first inverter stage are connected to each other.

4. The circuit of claim 2, wherein the second inverter stage is a transistor stage, and wherein the gate terminals of the transistors of the second inverter stage are connected to each other and wherein the drain terminals of the transistors are connected to each other.

5. The circuit of claim 2, wherein the gate terminals of the second inverter stage are connected to the gate terminals of the first inverter stage.

6. The circuit of claim 2, wherein the input terminal is connected to a source terminal of the second inverter stage.

7. The circuit of claim 2, wherein the output terminal is connected to a drain terminal of the second inverter stage.

8. The circuit of claim 2, wherein the additional circuit element is a transistor in saturated mode.

9. The circuit of claim 2, wherein the additional circuit element is a transistor in saturated mode where the gate of the transistor is connected to the VCC and the source is connected to ground whereby the defined signal is a high level signal.

10. The circuit of claim 2, wherein the additional circuit element is a transistor in saturated mode where the gate of the transistor is connected to the ground and the source is connected to VCC whereby the defined signal is a low level signal.

11. A digital circuit unit comprising an input terminal, a pull-up stage, a failsafe stage, a signal processing stage and an output terminal, wherein the failsafe stage comprises the features of claims 2 to 10.

ABSTRACT:

A method and a circuit for producing a failsafe output signal in case of an open circuit condition of an input pad of a digital circuit unit, comprising a first inverter stage (10, 18) providing a constant switch level; a second inverter stage (32, 44) providing a variable switch level that depends of the signal level of the input pad (28) and comparing the constant switch level of the first inverter stage (10, 18) to the variable switch level of the second stage (32, 44) and providing an output signal at an output terminal (42) thereof if the variable switch level of the second stage (32, 44) is greater than the constant switch level; and an additional circuit element (52) in series with the second inverter (32, 44) for decreasing the switching level of the second inverter stage (32, 44).

Fig. 2

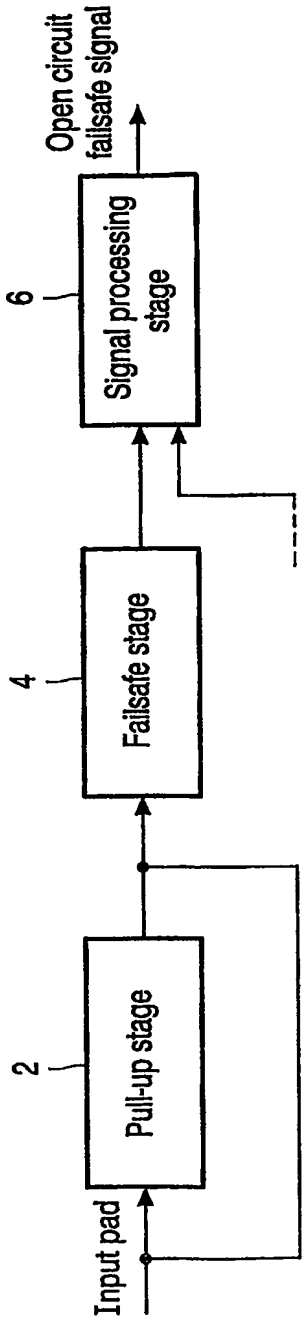
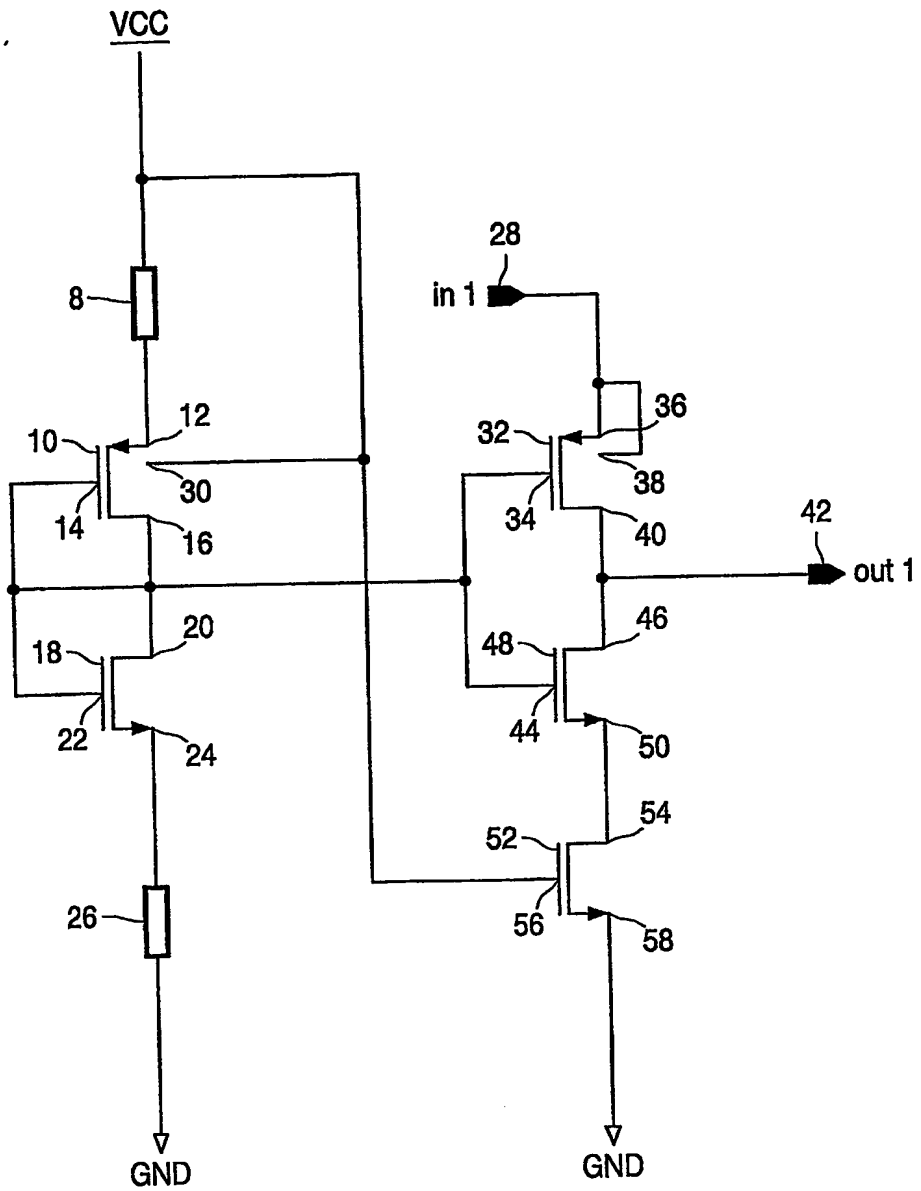


FIG. 1


VCC
8
28
in 1
10
12
30
14
16
32
36
38
34
40
42
out 1
18
20
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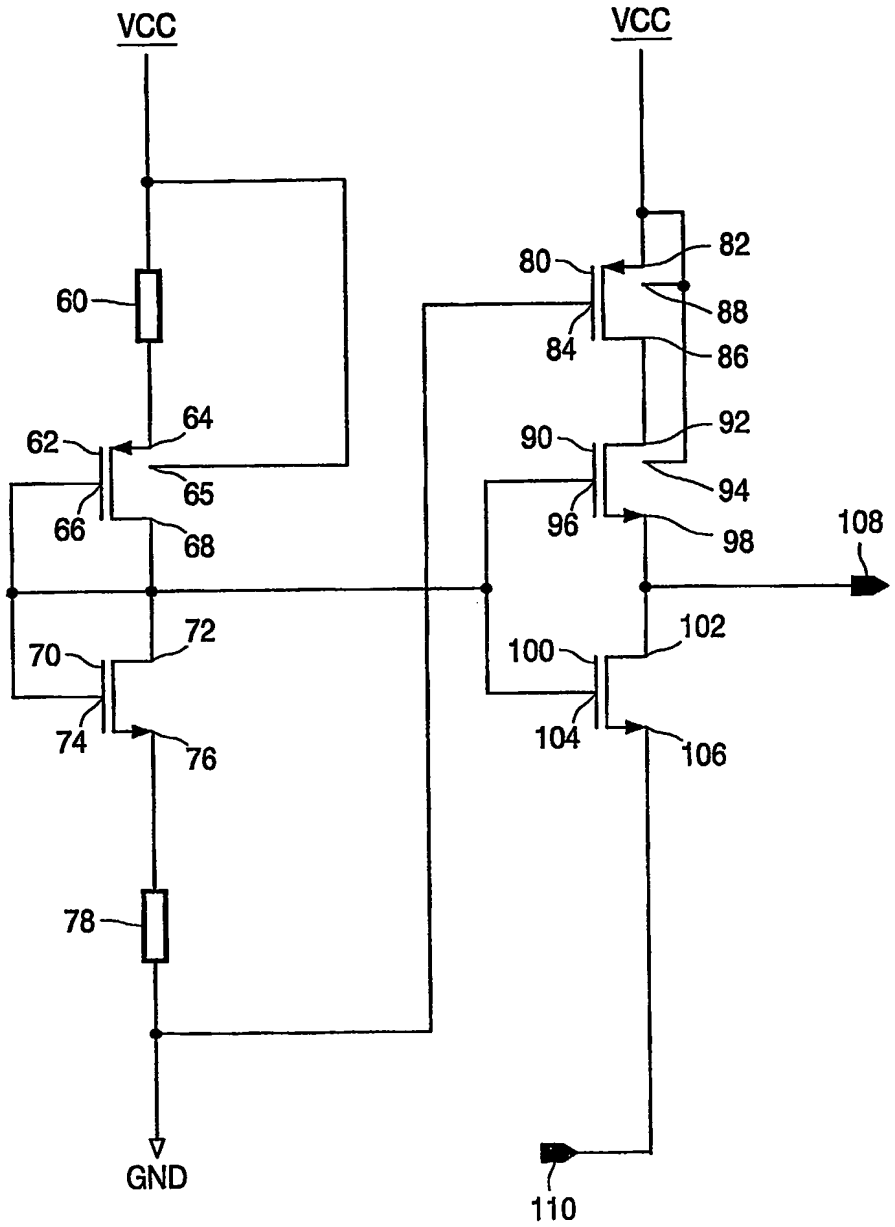
24
46
48
44
50
52
54
56
58
26
GND
GND

FIG. 2


VCC
VCC
60
62
64
65
66
68
70
72
74
76
78
GND
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86
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104
106
108
110

FIG. 3

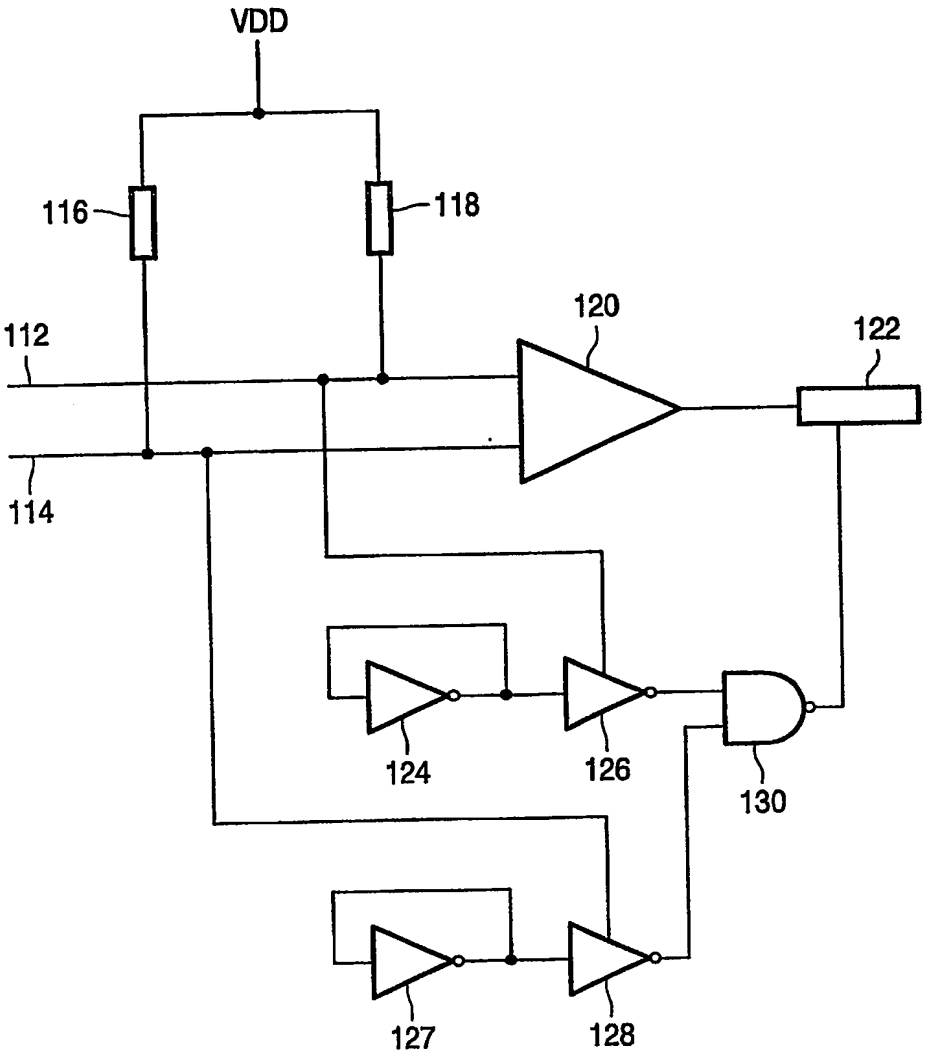

FIG. 4

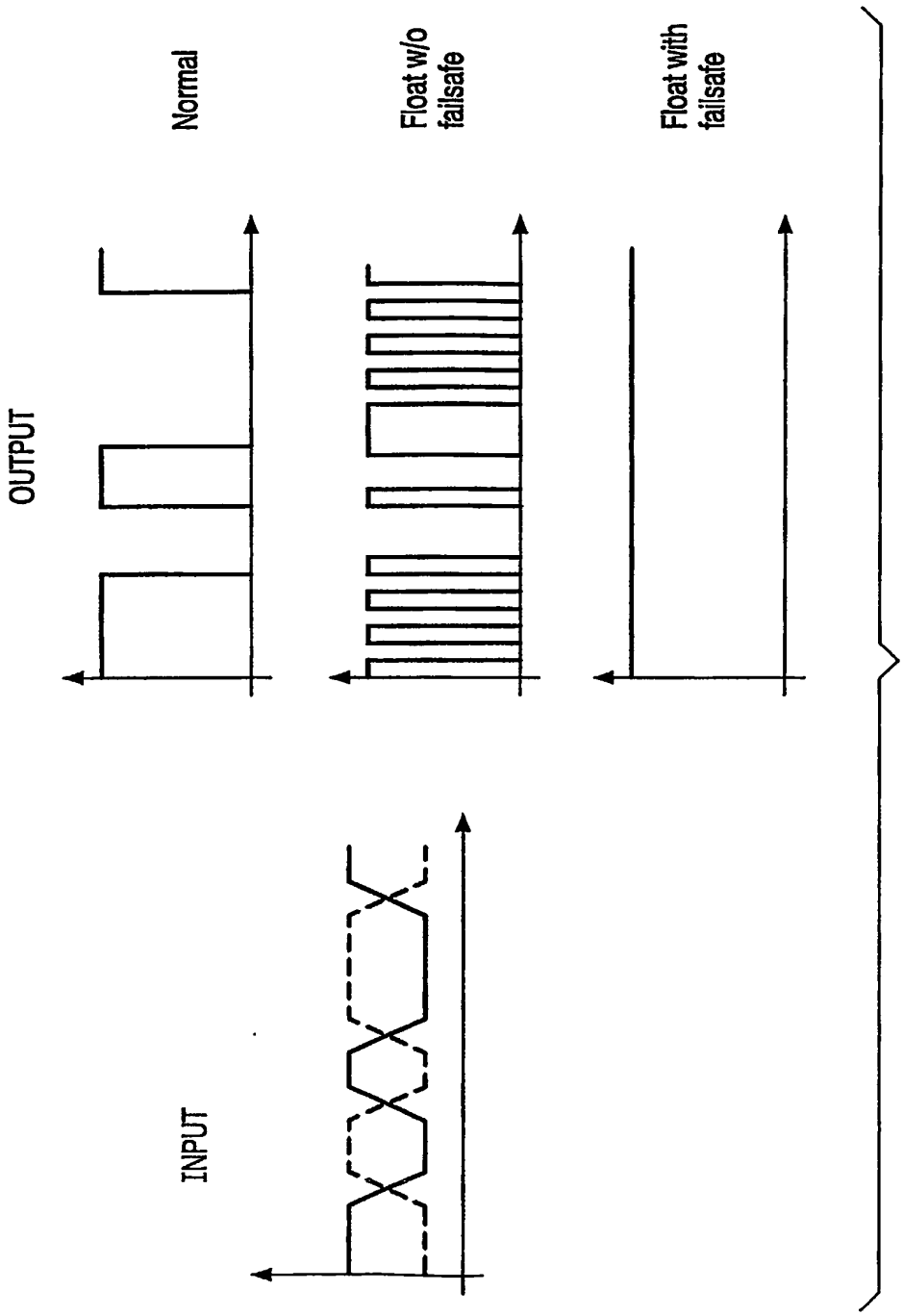

FIG. 5